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SEMICONDUCTOR ASSEMBLY & TEST - INTENSIVE ENGINEERING ACCELERATION PROGRAM



BY ELITE INDIGO

Walk away with practical 'quick wins' to effectively improve your Semiconductor Assembly skills and enhance productivity immediately.

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Semiconductor Assembly & Test - Intensive Engineering Acceleration Program

• Program Overview

This is a focused, high-impact engineering intensive designed to strengthen Assembly & Test technical capability while directly improving manufacturing productivity, yield stability, and operational performance.
In semiconductor assembly and test improvement teams, strong process understanding is essential to accurately identify and eliminate manufacturing wastes — including yield loss, downtime, speed inefficiencies, material overconsumption, rework, defect escape, and hidden factory losses.

By equipping engineers and manufacturing leaders with structured insight into process flow, parameter criticality, and system interdependencies, the program enables teams to detect performance gaps early, control variation effectively, and drive sustainable improvement across the assembly and test value chain.

• Learning Objectives

By the end of the course, participants will be able to learn about:

1. Understand the end-to-end semiconductor assembly and test process, including package architecture and yield stacking impact.
2. Identify critical process parameters and explain defect mechanisms across major back-end operations.
3. Interpret electrical test, inspection, and reliability data to diagnose manufacturing and field risks.
4. Apply contamination control, ESD management, and risk governance principles to prevent defect escapes.
5. Analyze productivity metrics such as OEE, bottlenecks, and yield losses to drive sustainable manufacturing performance improvement.

• Duration Two(2) Full-Day Workshop;

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• Course Schedule (Day 1)

DAY/TIME	Topic
1 Hour 30 Minutes	**Module 1: Semiconductor Ecosystem & Package Architecture** Learning Outcomes • Explain IDM vs Foundry vs OSAT structure. • Trace electrical & thermal path from silicon to PCB. • Differentiate package platforms (Leadframe vs Substrate, Others). Key Content • Global semiconductor value chain. • Die structure & pad layout. • Leadframe vs Substrate construction. • Package families: QFN, BGA, SOP, Power packages, Others. • Introduction to WLP / Advanced packaging exposure.
2 Hours	**Module 2: End-to-End Assembly Flow & Yield Stacking** Learning Outcomes • Describe complete back-end process sequence. • Explain output & CTQ for each station. • Understand cumulative yield stacking effect. • Relate upstream variation to downstream failure. Detailed Flow Coverage • Wafer mount, Dicing, Die attach, Wire bond, Ball attach. • Moulding, Marking, Trim & Form / Singulation, Plating. • AOI, Final Test, Packing. • Yield stacking math & COPQ implications. • Hidden factory concept.
1 Hour	**Lunch**

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• Course Schedule (Day 1) Cont.

DAY/TIME	Topic
2 Hours 30 Minutes	**Module 3: Critical Assembly Process Engineering** Learning Outcomes • Identify machine critical parameters. • Understand defect mechanism by process physics. • Interpret common failure signatures. • Link process settings to reliability risk. Engineering Focus Areas • Wafer Mount & Dicing: Blade thickness, spindle RPM, feed rate, coolant control, edge chipping & die crack. • Die Attach: Epoxy dispense system, bond line thickness, cure profile, voiding & die tilt. • Wire Bond: Capillary, ultrasonic power, loop profile control, NSOP & cratering. • Ball Attach: Flux printing, reflow profiling, solder integrity, voiding & bridging
1 Hour	**Module 4: Cleanroom, ESD & Risk Governance** Learning Outcomes • Explain contamination control strategy. • Identify ESD-sensitive failure modes. • Relate humidity to ESD risk. • Apply machine safety awareness. Key Topics • HEPA airflow concept. • ESD grounding ecosystem. • Wrist strap validation. • Moisture sensitivity & MSL exposure.
	Wrap-up and End

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• Course Schedule (Day 2)

DAY/TIME	Topic
1 Hour 30 Minutes	**Module 5: Molding, Marking & Mechanical Integrity** • Identify marking compliance requirements. • Understand trim/form tooling mechanics. • Recognize coplanarity failure risks. Content • Transfer pot & plunger system. • Clamp force & cure time. • Laser / Ink marking & traceability. • Coplanarity tolerance & bent lead defects.
2 Hours	**Module 6: Electrical Test Engineering Fundamentals** Learning Outcomes • Describe tester-handler integration. • Differentiate parametric vs functional test. • Interpret binning logic. • Understand guard band philosophy. Content • Loadboard & socket structure. • Electrical failure categories. • Handler alignment impact. • Test yield vs assembly yield relationship.
1 Hour	**Lunch**

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• Course Schedule (Day 2) Cont.

DAY/TIME	Topic
1 Hour	**Module 7: AOI, Visual Inspection & Defect Escapes** Learning Outcomes • Explain AOI algorithm logic. • Differentiate false call vs escape. • Classify visual defect types. Content • Lighting configuration. • Pattern recognition logic. • Escape prevention strategy.
1 Hour 30 Minutes	**Module 8: Reliability & Failure Mechanism Overview** Learning Outcomes • Understand common package reliability failures. • Interpret basic reliability tests. • Link assembly defects to field returns. Coverage • JEDEC reliability tests. • Moisture sensitivity & popcorn effect. • Wire bond fatigue & solder fatigue. • Thermal cycling exposure.
1 Hour	**Module 9: OEE, Bottleneck & Line Productivity Engineering** Learning Outcomes • Define Availability, Performance, Quality. • Identify bottleneck machine. • Calculate UPH impact. • Relate defect rate to OEE. Industrial Focus • OEE formula breakdown. • Downtime vs speed loss. • Quality loss vs scrap. • Throughput constraint thinking.
	Wrap-up and End

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ABOUT ELITE INDIGO

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