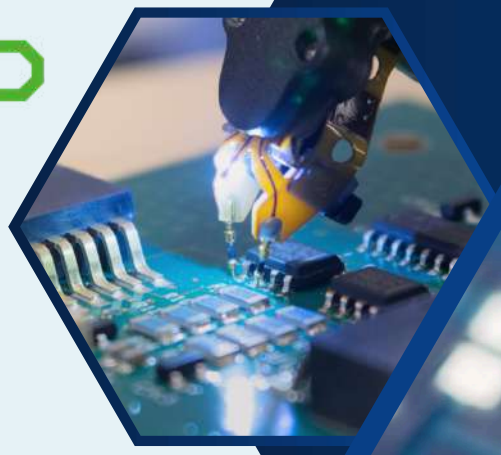
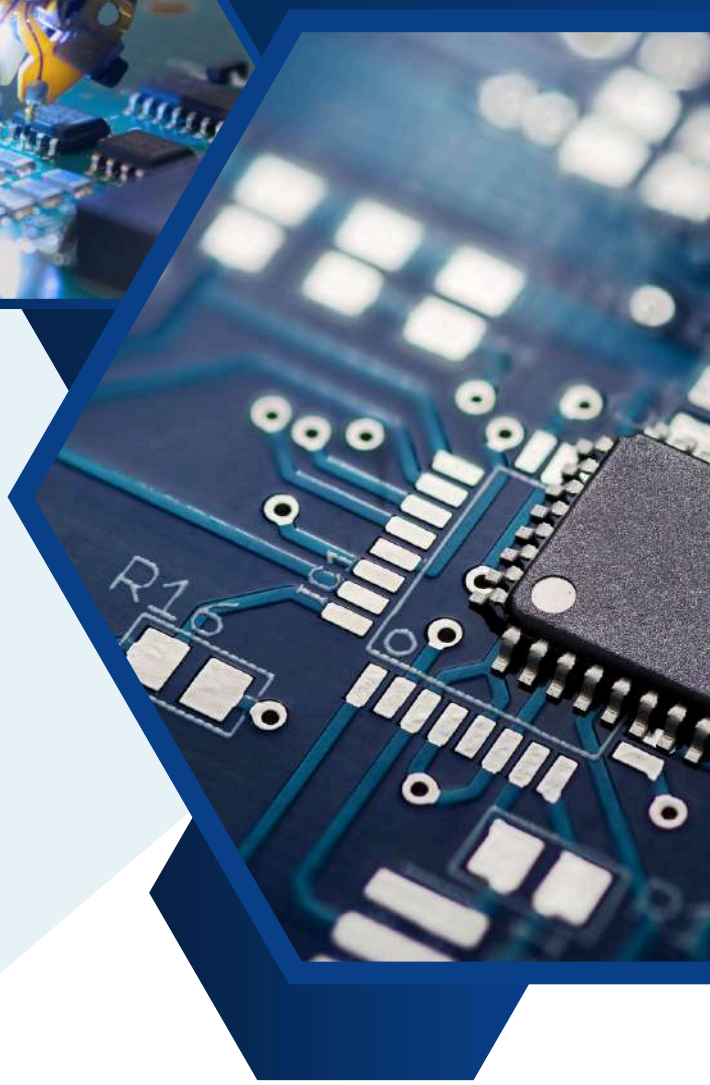
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# FROM SAND TO CIRCUIT: FULL SEMICONDUCTOR FABRICATION PROCESS

## BY ELITE INDIGO

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# From Sand to Circuit: Full Semiconductor Fabrication Process

## • Program Overview

This program provides participants with a comprehensive understanding of the semiconductor manufacturing journey, from silicon purification and wafer fabrication to assembly, testing, reliability, and failure analysis. The program explains how integrated circuits are created through photolithography, deposition, etching, packaging, and electrical testing while highlighting the critical relationship between process control, yield, quality, and product reliability. Through interactive activities, simulations, and industry case studies, participants will gain practical insights into both frontend and backend operations, enabling them to communicate effectively across semiconductor manufacturing functions and appreciate how modern electronic devices are produced and qualified.

## • Learning Objectives

By the end of the course, participants will be able to:

- Explain the complete semiconductor manufacturing flow from silicon purification to finished packaged devices.
- Describe the functions of major wafer fabrication processes, including oxidation, photolithography, etching, implantation, and deposition.
- Identify key assembly and test operations and their impact on product quality and manufacturing yield.
- Understand the purpose of reliability testing and failure analysis, and common semiconductor qualification requirements.

## • Duration

Two (2) Full-Day Workshop

# From Sand to Circuit: Full Semiconductor Fabrication Process

## Course Schedule (Day 1)

| DAY/TIME | DESCRIPTION |
|---|---|
| 2 Hours | **Module 1: Introduction to the Semiconductor Value Chain**<br>• Semiconductor industry overview, from sand to silicon<br>• Frontend vs Backend manufacturing<br>• Major device types (Discrete, Analog, Power, Logic, Sensors)<br>• **Learning Outcome:** Describe the end-to-end semiconductor manufacturing flow, Differentiate frontend and backend operations, Identify major semiconductor product categories<br>• **Activities:** Value Chain Mapping Exercise<br>  ◦ Teams arrange shuffled process cards into the correct semiconductor manufacturing sequence. |
| 2 Hours | **Module 2: Silicon Wafer Manufacturing**<br>• Silicon purification<br>• Czochralski crystal growth<br>• Ingot slicing, wafer lapping, polishing, and cleaning<br>• **Learning Outcome:** Explain how semiconductor-grade silicon is produced, Describe wafer manufacturing steps, Recognize critical wafer quality parameters<br>• **Activities:** Wafer Defect Identification<br>  ◦ Participants inspect sample wafer images and identify scratches, particles, pits, and edge defects. |
| 1 Hour | **Lunch** |
| 1 Hour 30 Minutes | **Module 3: Core Wafer Fabrication Processes**<br>• Oxidation, Photolithography & Etching<br>• Ion implantation & Thin film deposition (PVD/CVD)<br>• Planarization (CMP)<br>• **Learning Outcome:** Describe the purpose of each major wafer process, Explain how transistor structures are formed, Identify common process interactions<br>• **Activities:** Photolithography Simulation<br>  ◦ Teams use transparent masks to simulate pattern transfer and alignment challenges. |
| 1 Hour 30 Minutes | **Module 4: Yield, Defects & Process Control**<br>• Wafer maps & Yield calculation<br>• Defect density, Metrology & SPC basics<br>• Cleanroom contamination control<br>• **Learning Outcome**: Interpret basic wafer maps, Relate defects to yield loss, Understand the role of process control<br>• **Activities:** Yield Calculation Workshop<br>  ◦ Participants calculate yield using sample wafer data and identify the largest loss contributor. |
| | **Summary and End of Day 1** |

# From Sand to Circuit: Full Semiconductor Fabrication Process

## Course Schedule (Day 2)

| DAY/TIME | DESCRIPTION |
|---|---|
| 3 Hours | **Module 5: Semiconductor Assembly (Packaging)**<br>• Wafer sawing, Die attach & Wire bonding<br>• Molding & Lead finish<br>• Package types (QFN, BGA, SOIC, Power packages)<br>• **Learning Outcome:** Describe the complete assembly flow, Explain the purpose of major packaging processes, Recognize common package types<br>• **Activities:** Package Matching Challenge<br>  ◦ Teams match package types to their most suitable applications (automotive, power, mobile, sensors, etc.). |
| 1 Hour | **Lunch** |
| 2 Hours | **Module 6: Electrical Test & Product Qualification**<br>• Wafer probe, Final test & Burn-in<br>• Parametric testing<br>• Product qualification flow<br>• **Learning Outcome:** Differentiate wafer probe and final test, Explain why burn-in is performed, Understand qualification requirements<br>• **Activities:** Test Data Interpretation<br>  ◦ Participants review simplified test logs and determine pass/fail decisions. |
| 1 Hour | **Module 7: Reliability Engineering**<br>• Reliability concepts<br>• HTOL, Temperature cycling, HAST<br>• ESD & latch-up<br>• Automotive reliability requirements<br>• **Learning Outcome:** Explain the purpose of reliability testing, Identify major semiconductor stress tests, Relate failure mechanisms to reliability risks<br>• **Activities:** Reliability Test Selection Exercise<br>  ◦ Teams select appropriate reliability tests for a power device used in an electric vehicle. |
| 1 Hour | **Module 8: Failure Analysis Fundamentals**<br>• Failure analysis workflow<br>• Electrical localization, X-ray inspection<br>• Decapsulation, Cross-sectioning<br>• SEM/EDS overview<br>• Root cause determination<br>• **Learning Outcome**: Describe a structured FA investigation flow, Identify suitable FA techniques, Differentiate symptom, mechanism, and root cause<br>• **Activities:** Failure Analysis Case Study<br>  ◦ Participants analyze a real-world wire bond lift failure and propose the most probable root cause. |
| | **Summary and End of Course** |

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